

# Performance of Incoherent SAC-OCDMA Using a Burst-Mode Receiver with CDR and FEC

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**Abstract**— We demonstrate a 7×622 Mbps incoherent SAC-OCDMA system using a standalone receiver with CDR and FEC. We accomplish more than 2.5 dB coding gain, and error free transmission (BER < 10<sup>-9</sup>) for a fully loaded system.

## I. INTRODUCTION

Spectral amplitude-coded optical code-division multiple-access (SAC-OCDMA) is a good candidate for optical networks because of its ability to cancel multiple access interference (MAI), and to permit the use of low speed electronics operating at the bit rate [1]. Furthermore, advances in writing fiber Bragg gratings (FBGs) make possible the design of low cost and compact passive encoders/decoders well adapted to passive optical networks (PONs) [2]. Much research into OCDMA focuses on optical design, while assuming the availability of high-speed electronics [1], [2]. Emerging research is concerned with the electronic design of receivers for optical multi-access networks, featuring post-processing functionalities [3], [4]. Previous electronic receivers were reported in the literature for fast-frequency hop (FFH) OCDMA and PON systems [5], [6].

FFH-OCDMA (or  $\lambda$ -t OCDMA) requires electronics that operates at the chip rate rather than the data rate. SAC-OCDMA has the advantage of operating at the data rate, and enjoys excellent MAI rejection with balanced detection. In this paper we demonstrate experimentally an incoherent SAC-OCDMA system supporting seven asynchronous users at 622 Mbps (FFH results were at 155 Mbps data rate) with no global clock, i.e., using a standalone receiver with a commercial SONET clock-and-data recovery (CDR); forward-error correction (FEC) is also implemented on a field programmable gate array (FPGA). We quantify the increase in soft capacity via FEC, while working with a non-ideal recovered clock that provides realistic, achievable sampling.

## II. SAC-OCDMA SYSTEM ARCHITECTURE

A simplified block diagram of the SAC-OCDMA system is shown in Fig. 1. A shared incoherent broadband source is filtered around 1542.5 nm using two cascaded FBG band-pass filters providing a 9.6 nm band. The light is then modulated with a non-return-to-zero 2<sup>15</sup>-1 PRBS using a polarization independent electro-absorption modulator. The desired information rate per user is 622 Mbps; an RS(255,239) code introducing 15/14 of overhead leads to an aggregate bit rate of

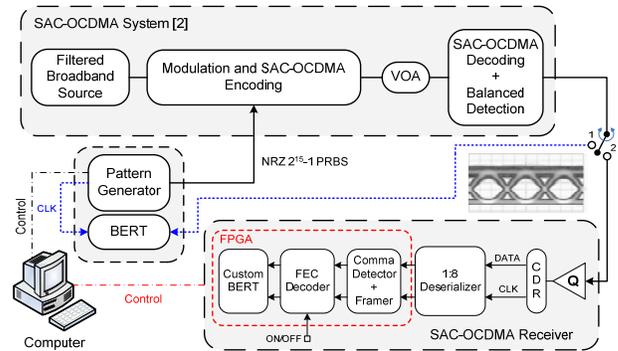


Fig. 1. Simplified SAC-OCDMA experimental setup with burst-mode receiver (BERT: BER tester, CLK: Clock, NRZ: non-return-to-zero, PRBS: pseudo random binary sequence, Q: quantizer, and VOA: variable optical attenuator).

666.43 Mbps. The modulated signal is then spectrally encoded using 7 FBGs (corresponding to 7 users) working in transmission; balanced incomplete block design codes with length 7 and weight 3 are used as the user signature codes [2]. After encoding, signals from different users are delayed differently with optical delay lines to decorrelate the data, and then combined on a single fiber. At the receiver side a variable attenuator is used to control the received power. Two FBGs also working in transmission are used to decode the desired user prior to balanced photo-detection [2]. The output of the balanced photo-detector is then amplified and low-pass filtered by a 4<sup>th</sup> order Bessel-Thomson filter whose cutoff frequency is 467 MHz. Such a filter reduces intensity noise from the incoherent broadband source [7], while keeping intersymbol interference to a minimum. Bit error rate (BER) measurements are then performed with either a global clock, or through our OCDMA receiver, corresponding to either option '1' or option '2', respectively (Fig. 1).

## III. BURST-MODE RECEIVER DESIGN

In Fig. 1 we see the main building blocks of the OCDMA receiver: a multi-rate SONET CDR from Analog Devices, a 1:8 deserializer from Maxim-IC, and a FEC RS(255,239) decoder implemented on a Virtex II FPGA from Xilinx. The receiver structure is similar to that in [5].

A quantizer is used before the CDR to apply a certain threshold on the incoming signal in order to filter out intensity noise. The threshold was manually adjusted to sample in the middle of the eye opening, to obtain the optimum BER.

The multi-rate CDR then recovers the clock and data from the incoming signal. It is operated at either 622 Mbps or 666.43 Mbps depending on whether the FEC is OFF or ON, respectively. The CDR is followed by a 1:8 deserializer that reduces the frequency of the recovered clock and data to a frequency that can be processed by the digital logic.

On the FPGA, automatic detection of the payload is implemented through a comma detector and a framer. A personal computer (PC) was used to control the output of the pattern generator and to communicate with the FPGA on the receiver. The RS(255,239) decoder is turned on for the BER measurements with FEC, otherwise it is by-passed. The FPGA-based BERT is then used to measure the BER. This eliminates the need to up convert the frequency back to 622 Mbps or 666.43 Mbps using an 8:1 serializer after the FPGA, and hence avoids the use of a commercial BERT.

#### IV. RESULTS AND DISCUSSION

The BER curves for 1, 3, 5, and 7 simultaneous users for both the global clock and the recovered clock are illustrated in Fig. 2. The horizontal axis represents the useful power, in other words the received power from the desired user. The corresponding eye diagrams at -18 dBm are also shown. Note that error free transmission (BER) is achieved only for up to 5 simultaneous users. A BER floor at  $\sim 10^{-6}$  is reached for 7 users because of the intensity noise added by the MAI as seen from the eye diagrams [7]. It can also be inferred that a negligible penalty (less than 0.25 dB at  $\text{BER} = 10^{-9}$ ) is added due to the non-ideal sampling of the CDR. It is important to add that at power levels smaller than -26 dBm we were able to accurately control manually the decision threshold (using a DC power supply) for the CDR measurements, compared to the use of the automated decision threshold in the BERT for global clock measurements. The manual optimization explains the slight improvement in the performance when using the recovered clock at lower power levels.

In Fig. 3 we plot the BER versus useful power when using both CDR and FEC options; the previous results (using only CDR) are also plotted for convenience and for comparison. Error free transmission ( $\text{BER} < 10^{-9}$ ) is achieved for all 7 users. A coding gain of more than 2.5 dB, 2.7 dB, and 5 dB (measured at  $\text{BER} = 10^{-9}$ ) for 1 user, 3 users, and 5 users, respectively, is achieved. Furthermore, the BER floor for 7 users is eliminated.

#### V. CONCLUSION

We experimentally evaluated the performance of a realistic  $7 \times 622$  Mbps incoherent SAC-OCDMA system using a burst-mode receiver featuring automatic detection of payload, CDR, and RS(255,239) FEC. The effect of intensity noise and other impairments was significantly reduced. Error free transmission was achieved for a fully loaded system; coding gain of more than 2.5 dB was measured.

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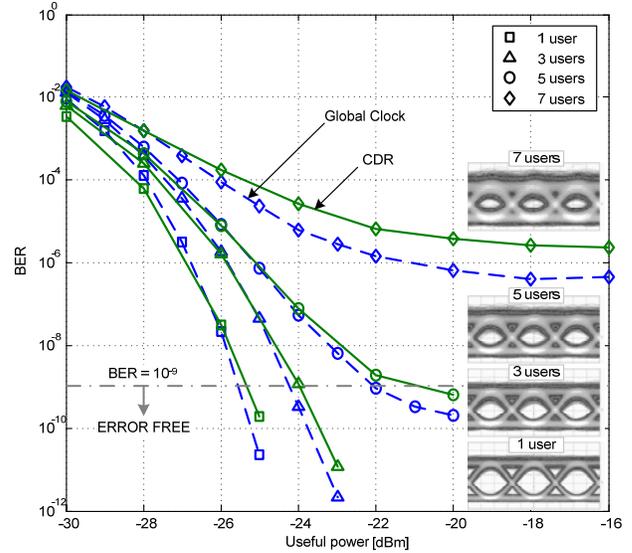


Fig. 2. BER vs. useful power for different number of users (Dashed lines: using the global clock, solid lines: using CDR).

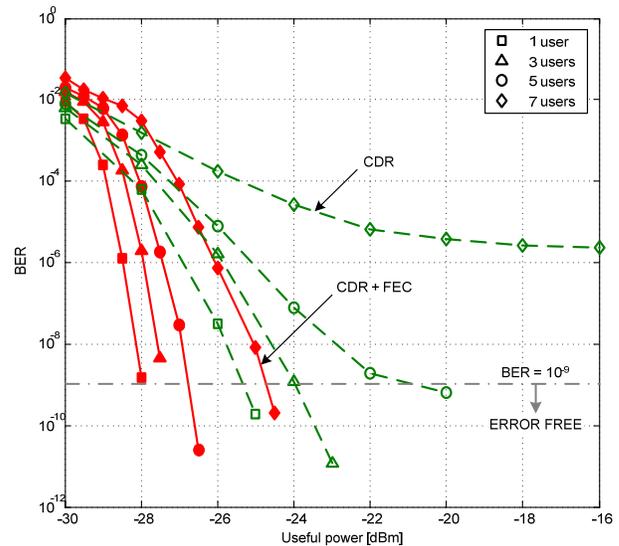


Fig. 3. BER vs. useful power for different number of users (Dashed lines: using CDR, solid lines: using CDR and FEC).

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